Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Supplementary Examinations, November -2019

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A (22 Marks)

1. a) List the properties of DT system. [3M]
   b) Find and plot the spectrum of $\delta(n-1)$. [4M]
   c) Find the IZT of $X(z) = \frac{z}{z-1}$, for $|z| > 1$ and $|z| < 1$. [4M]
   d) Explain the mapping of s-plane to z-plane in impulse invariant transformation. [4M]
   e) Give the schematic representation of decimator and interpolator. [4M]
   f) What are the important features of programmable digital signal processor? [3M]

PART –B (48 Marks)

2. a) Discuss the stability of the systems described by the impulse response below: [8M]
      i. $h(n) = 2^{-n}u(n)$.
      ii. $h(n) = 0.5^{n}u(n) - 0.5^{n}u(4-n)$.
   b) Determine the steady-state response of the system governed by the following difference equation: $12y(n) - 7y(n-1) + y(n-2) = \sin(\frac{\pi}{3}n)\, u(n)$. [8M]

3. a) Compute the coefficients of the Fourier series of the periodic sequence given below and plot its spectrum. $x(n) = \sin(\frac{2\pi n}{N}), for\ N = 20$. [8M]
   b) Compute the 8-point DFT of the following sequence using radix-2 DITFFT algorithm: $x(n) = \delta(n) + 2\delta(n-1) - \delta(n-2) + \delta(n-3)$. [8M]

4. a) Compute the time response of the causal system described by the transfer function $H(z) = \frac{(z-1)^2}{z^2-0.32z+0.8}$ when the input signal is the unit step. [8M]
   b) Give the direct form-I and direct form-II realizations for the transfer function: [8M]
   $$H(z) = 0.0034 + 0.0106z^{-2} + 0.0025z^{-4} + 0.0149z^{-6}.$$

5. a) Distinguish between FIR and IIR filters. [8M]
   b) What are the analog to digital filter transformation techniques? Explain. [8M]

6. a) What is the difference between single-rate and multi-rate systems? Explain with examples. [8M]
   b) Give the frequency domain description of up-sampler. [8M]

7. Write notes on the following:
   a) Specialized addressing modes. [8M]
   b) TMS320C5x bus structure. [8M]

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Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Supplementary Examinations, November -2018

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Test the given system for time invariance : $y(n) = n\,x(n)$.	[3M]
	b)	State any four properties of DFT	[4M]
	c)	Find the Z-transform of $x(n) = (1/8)^n\ u(n)$ and its ROC.	[4M]
	d)	Draw the direct form structure of $y(n) = \sum_{K=0}^{N-1} h[k]x[n-k]$	[4M]
	e)	What is the significance of Multirate Signal processing? What are the applications	[3M]
	f)	What are the differences between fixed point processors and floating point Processors?	[4M]

PART -B

2	a)	Find the solution to the following linear constant coefficient difference equation with initial conditions $y(-1)=4\ and\ y(-2)=10$ $y(n)-\frac{3}{2}y(n-1)+\frac{1}{2}y(n-2)=\left(\frac{1}{2}\right)^n\ for\ n\geq 0$	[8M]
	b)	Explain the frequency domain representation of Discrete time signals	[8M]
3	a)	Given $x(n)=\{1,2,3,4,4,3,2,1\}$, find $X(k)$ using DIF FFT algorithm.	[8M]
	b)	State and prove time – shifting and time scaling property of DFT.	[8M]
4	a)	Determine the ZT of $x[n] = -na^n u[-n-1]$.	[8M]
	b)	What are the basic structures of FIR systems? Explain	[8M]
5	a)	What are the effects of windowing? Comparing various windowing techniques.	[8M]
	b)	Design a High Pass FIR filter whose cut-off frequency is 1.2 radians/sec and N = 9 using Hamming Window.	[8M]
6	a)	Derive the frequency domain representation of decimator.	[8M]
	b)	Explain the following terms: i) Up – sampling ii) Down- sampling	[8M]
7	a)	What is MAC? Explain its operation in detail.	[8M]
	b)	Explain about Special addressing modes	[8M]

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Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Supplementary Examinations, November/December-2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) What is BIBO stability? What are the conditions for BIBO stability? [3M]
b) Distinguish between linear and circular convolutions of two sequences. [4M]
c) Define canonic and non-canonic structures. [4M]
d) Explain Gibb's phenomenon. [4M]
e) Show that the interpolator is a time-variant system. [3M]
f) Write down the applications of each of the families of TIs DSPs. [4M]

PART -B

2 a) Explain the method of obtaining the frequency response of linear shift-invariant systems. [4M]
b) For the following discrete time signals, determine whether or not the system is linear, shift invariant, causal and stable. [8M]
(i) y(n)=x(n+7) (ii) y(n)= x^3(n)
c) Determine the magnitude and phase response of the following system: [4M]
y(n)=[x(n) + x(n-1)]/2.

3 a) State shifting property of the DFT. [3M]
b) Compute the FFT for the sequence x(n)= n^2+1 where N=8 using DIT algorithm. [8M]
c) What is DIT FFT algorithm? [5M]

4 a) How will you develop a cascade structure with direct form II realization of a sixth order IIR transfer function? [7M]
b) Realize an FIR filter with impulse response is given by [9M]

$$h(n) = (1|2)^n[u(n) - u(n-5)]$$

5 a) Compare bilinear transformation and other transformations based on their stability. [7M]
b) The desired frequency response of a low-pass filter is [9M]

$$H_d(e^{j\omega}) = \begin{cases} e^{-j3\omega}, & -\frac{3\pi}{4} \le \omega \le \frac{3\pi}{4} \\ 0, & 3\pi/4 < |\omega| \le \pi \end{cases}$$

Determine $H(e^{j\omega})$ for M=7 using a rectangular window.

6 a) Discuss the computationally efficient implementation of interpolator in an FIR filter. [8M]
b) Draw and explain the polyphase structure of a decimator. [8M]

7 a) List the family members of the first generation TMS processor and note down the distinguished features. [7M]

b) List the enhanced features of the TMS320C5X processor. [9M]

Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Supplementary Examinations, April/May -2019

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What are the conditions for stability and causality of an LSI system?	[4M]
	b)	Define DFT and IDFT	[3M]
	c)	Find the z transform of $x[n] = \sin s [\omega_o n]\, u[n]$.	[4M]
	d)	What is the necessary and sufficient condition for linear phase Characteristics of an FIR filter?	[4M]
	e)	What is meant by aliasing? How to avoid it?	[3M]
	f)	What are the advantages of VLIW architecture?	[4M]

PART -B

2	a)	Determine the frequency response, and time delay of the systems given by $y(n)-\frac{1}{2}y(n-1)=x(n)$	[8M]
	b)	What is the significance of convolution? Explain	[8M]
3	a)	Compute the DFTs of the sequence $x(n)=2^{-n}$, where N = 8 using DIT algorithm.	[8M]
	b)	State any four properties of DFS and prove them	[8M]
4		Realize the following IIR system in the direct form I, direct from II and parallel forms. $H(z)=1/(1+az^{-1})(1-bz^{-1})$	[16M]
5	a)	The desired frequency response of a low pass filter is $H_d(e^{jw})=\begin{cases}1; \frac{-\pi}{2}\le w\le\frac{\pi}{2}\\ 0; \frac{\pi}{2}\le w\le\pi\end{cases}$ Determine $h_d(n)$ *for* $M = 7$ using a rectangular window	[8M]
	b)	Explain FIR filter design using windowing method.	[8M]
6	a)	Explain the following terms: i) Decimation ii) interpolation.	[8M]
	b)	What are the applications of Multi rate system? Explain.	[8M]
7	a)	What are the various addressing modes used in the TMS320C5X processor?	[8M]
	b)	What are the limitations of pipelining in Digital Signal Processor?	[8M]

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What are the elementary discrete time signals?	[3M]
	b)	Find the IDFT of Y (k) = (1, 1, 1, 0)	[4M]
	c)	State the properties of ROC.	[4M
	d)	Why IIR filters do not have linear phase?	[3M]
	e)	Explain how a multi-rate system is different from a single-rate system?	[4M]
	f)	Explain the basic architectural features of programmable DSP devices.	[4M]

PART -B

2	a)	Find the periodicity of the signal $x(n) = \sin(2\pi n / 3) + \cos(\pi n / 2)$	[4M]
	b)	Explain the frequency response of discrete time system.	[8M]
	c)	What is the causality condition for an LTI system?	[4M]
3	a)	Find the DFT of $x[n] = a^n$ for $0 \le n \le 3$ $= 0$ otherwise.	[8M]
	b)	Find the linear convolution of the sequences x[n]={ 1,4,0,9,-1} and h[n]= {-3,-4,0,7}	[8M]
4	a)	State and prove any three properties of Z- Transform.	[8M]
	b)	Obtain direct form I, direct form II and cascade realizations of system described by the equation, y[n]=y[n-1]-(1/2)y[n-2]+x[n]-x[n-1]+x[n-2]	[8M]
5	a)	Determine the system function H(Z) of the lowest order Chebyshev digital filter that meets the following specifications. i) 3 db ripple in the passband $0 \le \lvert\omega\rvert \le 0.3\pi$ ii) At least 40 dB attenuation in the stopband $0.35\pi \le \lvert\omega\rvert \le \pi$. Use the bilinear transformation.	[8M]
	b)	Explain the need for the use of window sequence in the design of FIR filter. Describe the window sequence generally used and compare the properties.	[8M]
6	a)	What is Interpolation? Explain about the frequency domain description of an Interpolator.	[8M]
	b)	What do you mean by fractional sampling rate conversion? Explain with an example of converting 48 kHz signal to 44.1 kHz signal using multi-stage fractional sampling rate converter.	[8M]
7	a)	Discuss in detail the Basic Architectural features of programmable DSP devices,	[8M]
	b)	Discuss in detail the Pipeline Operation of TMS320C54XX Processors.	[8M]

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Define discrete time signal and give examples.	[3M]
	b)	What are the advantages FFT over DFT.	[4M]
	c)	What are the different methods of evaluating inverse z transform?	[3M]
	d)	Draw the indirect form realizations of FIR systems?	[4M]
	e)	Derive transfer function of an Interpolator.	[4M]
	f)	Discuss about the various sources of errors in the computation using DSP processor implementations.	[4M]

PART -B

2	a)	Discuss the frequency domain representation of linear time-invariant systems.	[8M]
	b)	Determine the frequency response for the system given by y(n)-3/4y(n-1)+1/8 y(n-2) = x(n)- x(n-1)	[8M]
3	a)	Find the DFT of the sequence x[n]={1,2,1,2,1,2,1,2} using decimation in time algorithm.	[8M]
	b)	State and prove any four Properties of discrete Fourier series.	[8M]
4	a)	With respect to Z transforms define the properties of ROC.	[8M]
	b)	Obtain the parallel form realization for the IIR system described by the transfer function $H(z) = \frac{3 + 3.6z^{-1} + 0.6z^{-2}}{1 + 0.1z^{-1} - 0.2z^{-2}}$.	[8M]
5	a)	Convert the following analog transfer function in to digital using bilinear transform and IIT methods with T=1sec $H(s) = \frac{s}{(s+3)(s+9)}$	[8M]
	b)	Design a HPF of length 7 with cut off frequency of 2 rad/sec using Hamming window..	[8M]
6	a)	With necessary derivations explain the operation of sampling rate conversion by a factor of I/D in both frequency and time domains.	[8M]
	b)	What are the applications of multirate digital signal processing?	[8M]
7	a)	Explain the various pipeline programming models that are adapted in DSP processors.	[8M]
	b)	Explain the Bus Architecture of DSP Processor.	[8M]

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2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Determine whether the following system given by y(n) = log10[{x(n)}] is Casual or not.	[3M]
	b)	What are the properties of convolution sum?	[4M]
	c)	List the applications of Z – transforms.	[3M]
	d)	Compare Chebyshev Filter and Butterworth Filter.	[4M]
	e)	Derive transfer function of Decimator.	[4M]
	f)	What are the functional units present in the TMS320C54XX processor?	[4M]

PART -B

2	a)	Consider a signal $x[n]=(-a)^{-n}\,u[n]$ determine the spectrum X(w).	[8M]
	b)	Determine the response of Second order Discrete Time system governed by the difference equation y(n)-2y(n-1)-3y(n-2)= x(n)+4x(n-1), n≥0,when the input signal is $x(n)= 2^n u(n)$, with initial conditions y(-2)=0,y(-1)=5.	[8M]
3	a)	Explain the significance of FFT algorithms. Draw the basic butterfly diagram for radix - 2 DIT-FFT.	[8M]
	b)	Find the DFT of x[n]={0.5,0.5,0.5,0.5,-1,-1,-1,-1} using decimation in time algorithm.	[8M]
4	a)	Find the Z-Transform $x[n] = (\frac{1}{3})^n Sin[\frac{\pi}{4}n]\,u[n]$.	[8M
	b)	Realize $H(z) = \frac{1 + 0.6z^{-2} + 0.2z^{-1}}{3 + 5z^{-1} + 4^{-2}}$ using Direct form I and Direct form II structures	[8M
5	a)	Distinguish between ”maximally flat magnitude response” and “equiripple magnitude response” filters.	[8M
	b)	Explain the impulse invariance method of IIR filter design.	[8M
6	a)	Explain the concept of multi rate signal processing along with two applications of it	[8M
	b)	Explain how sampling rate conversion of band pass signals can be achieved.	[8M
7	a)	Explain in detail the circular addressing mode and bit-reversed addressing mode.	[8M
	b)	Explain Memory Access schemes in DSPs.	[8M

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2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1 a) Determine whether the system defined by $y(n) = x(-n^2-2)$ is time invariant or not. [3M]

b) What is FFT? How many multiplications and additions are required to compute N point DFT using redix-2 FFT? [4M]

c) State and prove Parsvel's theorem. [4M]

d) Why FIR filters are always stable? [4M]

e) What is Down sampling? [3M]

f) Explain the role of on-chip peripherals for programmable digital signal processors. [4M]

PART -B

2 a) For each case determine the system is stable or causal [10M]
i) $h(n)= \sin(\pi n / 2)$ ii) $h(n) = \delta(n) + \sin \pi n$ iii) $h(n) = 2^n u(-n)$

b) Show that an LTI system can be described by its unit sample response. [6M]

3 a) State and prove convolution Properties of DFT. [8M]

b) Compute the DFT for the sequence (0.5,0.5,0.5,0.5,1,1,1,1) using DIF-FFT [8M]

4 a) Find the Inverse Z-Transform of $X(z) = \frac{1 - \frac{1}{3} z^{-1}}{(1 - z^{-1})(1 + 2z^{-1})}, |z| > 2$ using partial fractions method. [8M

b) Obtain the cascade form realization for the recursive IIR system described by the transfer function $H(z) = \frac{3 + 3.6z^{-1} + 0.6z^{-2}}{1 + 0.1z^{-1} - 0.2z^{-2}}$. [8M

5 a) Explain the design procedure for IIR filters using Butterworth approximations. [8M

b) A low pass filter is to be designed with the following desired frequency response. [8M

$H_d(e^{jw}) = e^{-j2w}, -\pi/4 \le \omega \le \pi/4$
$0, \quad \pi/4 \le |\omega| \le \pi$

Determine the filter coefficients $h_d(n)$ if the window function is defined as

$\omega(n) = 1, \quad 0 \le n \le 4$
$0, \quad$ otherwise

Also determine the frequency response $H(e^{jw})$ of the designed filter.

6 a) With the help of an example define Decimation and Interpolation operations in DSP. [8M]

b) A signal, x(n), at a sampling frequency of 2.048 kHz is to be decimated by a factor of 32 to yield a signal at a sampling frequency of 64 Hz. The signal band of interest extends from 0 to 30 Hz. The anti-aliasing digital filter should satisfy the following specifications: [8M]

Pass band deviation	0.01 dB
Stop band deviation	80dB
Pass band	0-30Hz
Stop band	32-64 Hz

The signal components in the range from 30 to 32 Hz should be protected from aliasing. Design a suitable two stage decimator.

7 a) What is the difference between internal and external modes of clocking of TMS320C54XX Processor? [8M]

b) Explain different pipeline programming models that are adapted in DSP processors? [8M]

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Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Regular/Supplementary Examinations, April - 2017

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Test whether the following signal is periodic or not ,if periodic find the fundamental period $\sin\sqrt{2}\,\pi\, t$	[4M]
	b)	Find the DFT of a sequence x(n) ={1 ,1, 2, 2}	[4M]
	c)	Give block diagram representation of linear constant-coefficient difference equations.	[4M]
	d)	By impulse invariant method obtain the digital filter transfer function and the differential equation of the analog filter h(s) =1/s+1	[4M]
	e)	What are the applications of multi rate DSP?	[3M]
	f)	List special feature of DSP architecture.	[3M]

PART -B

2	a)	Determine whether each of the following systems defined below is (i) casual (ii) linear (iii) dynamic (iv) time invariant (i) $y(n) = \log_{10}[\{x(n)\}]$ (ii) $y(n) = x(-n-2)$ (iii) $y(n) = \cosh[nx(n) + x(n-1)]$	[12M]
	b)	Give the frequency domain representation of discrete time signals.	[4M]
3	a)	Compute the DFT for the sequence {1, 2, 0, 0, 0, 2, 1, 1}. Using radix -2 DIF FFT and radix -2 DIT- FFT algorithm.	[8M]
	b)	Derive the equation to implement a butterfly structure In DITFFT algorithm.	[8M]
4	a)	Realize the filter $H(z)=(z^{-1}-a)(z^{-1}-b) / (1-az^{-1})(1-bz^{-1})$ in cascade and parallel forms.	[8M]
	b)	State and prove time convolution property of Z-Transforms.	[8M]
5	a)	Obtain the impulse response of digital filter to correspond to an analog filter with impulse response $h_a(t) = 0.5\, e^{-2t}$ and with a sampling rate of 1.0kHz using impulse invariant method.	[8M]
	b)	Compare bilinear transformation and impulse invariant mapping.	[8M]
6	a)	Explain the decimation and interpolation process with an example. Also find the spectrum.	[8M]
	b)	The sequence x(n)=[0,2,4,6,8] is interpolated using interpolation sequence b_k =[1/2,1,1/2] and the interpolation factor is 2.find the interpolated sequence y(m).	[8M]

7 a) Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram. [8M]

b) What are interrupts? What are the classes of interrupts available in the TMS320C5xx processor? [8M]

Code No: RT32042 **R13** SET - 2

III B. Tech II Semester Regular/Supplementary Examinations, April - 2017

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Test whether the following signal is periodic or not ,if periodic find the fundamental period sin20 πt+sin5πt	[4M]
	b)	Find the values of WNk, When N=8, k=2 and also for k=3.	[4M]
	c)	Draw the direct form realization of FIR system.	[4M]
	d)	What are the properties of chebyshev filter?	[3M]
	e)	Find the spectrum of exponential signal decimated by factor 2.	[4M]
	f)	What are the advantages of VLIW architecture?	[3M]

PART -B

2	a)	Determine the impulse response of the filter defined by y(n)=x(n)+by(n-1).	8M]
	b)	A system has unit sample response h(n) given by h(n)=-1/δ(n+1)+1/2δ(n)-1-1/4 δ(n-1). Is the system BIBO stable? Is the filter causal? Justify your answer.	[8M]
3	a)	Find the DFT of the sequence x[n]={1,2,3,4,5,6,7,8}.	[8M]
	b)	Explain the use of FFT algorithms in linear filtering and correlation.	[8M]
4	a)	Determine the cascade and parallel realization for the system transfer function $H(z) = 3(z^2+5z+4) / (2z+1)(z+2)$.	[8M]
	b)	State and prove frequency convolution property of Z-Transforms.	[8M]
5	a)	Design an ideal high pass filter with a frequency response Hd (ejw) = 1 for $\pi/4 \leq \lvert w \rvert \leq \pi$ = 0 for $\lvert w \rvert \leq \pi/4$ Find the values of h(n) for N = 11 using Hamming window. Find H (z) and determine the magnitude response.	[8M]
	b)	Derive the expression for Bi linear Transform.	[8M]
6	a)	Explain the operation used in DSP to increase the sampling rate.	[8M]
	b)	The sequence x(n)=[0,2,4,6,8] is interpolated using interpolation sequence bk =[1/2,1,1/2] and the interpolation factor is 2.find the interpolated sequence y(m).	[8M]
7	a)	Explain the different types of interrupts in TMS320C54xx Processors.	[8M]
	b)	Describe any four data addressing modes of TMS320c54xx processor.	[8M]

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Code No: RT32042 **R13** SET - 3

III B. Tech II Semester Regular/Supplementary Examinations, April - 2017

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Test the following systems for time invariance $y(n)=n\,x^2(n)$	[4M]
	b)	Define DFT and IDFT	[4M]
	c)	What are the applications of Z-Transforms?	[4M]
	d)	What are the advantages of Kaiser widow?	[4M]
	e)	What are "decimation" , “decimation factor “and "down sampling"?	[3M]
	f)	List the on-chip peripherals	[3M]

PART -B

2	a)	Determine and sketch the magnitude and phase response of the following systems (i) $y(n) = 1/3\,[x(n) + x(n-1) + x(n-2)]$ (ii) $y(n) = ½[x(n) – x(n-1)]$ (iii) $y(n) - 1/2y(n-1)=x(n)$	[12M]
	b)	Determine the impulse response of the filter defined by $y(n)=x(n)+by(n-1)$.	[4M]
3	a)	Determine IDFT of the following (i) $X(k)=\{1,1-j2,-1,1+j2\}$ (ii)$X(k)=\{1,0,1,0\}$	[8M]
	b)	Find the DFT of the sequence $x[n]=\{1,2,3,4,5,6,7,8\}$ using DITFFT.	[8M]
4	a)	Obtain the direct form I, direct form II and Cascade form realization of the following system functions. $Y(n) = 0.1\,y(n-1) + 0.2\,y(n-2) + 3x(n) + 3.6\,x(n-1) + 0.6\,x(n-2)$.	[8M]
	b)	Explain Transposed forms.	[8M]
5	a)	Comparison of FIR and IIR filters.	[8M]
	b)	What is Hamming Window function? Obtain its frequency domain characteristics.	[8M]
6	a)	What is Multi Rate Signal Processing? Explain any two applications of multirate signal processing.	[8M]
	b)	Derive the Frequency domain Transfer function of a Decimator.	[8M]
7	a)	List the major architectural features used in DSP system to achieve high speed program execution.	[8M]
	b)	With examples explain the different addressing formats supported by DSP processors for various signal processing applications.	[8M]

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Code No: RT32042 **R13** SET - 4

III B. Tech II Semester Regular/Supplementary Examinations, April - 2017

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Test the following systems for time invariance a $^{x(n)}$.	[3M]
	b)	What are the advantages of FFT over DFT.	[4M]
	c)	Find the Z-transform of x(n)= $(1/8)^n$ u(n) and its ROC.	[4M]
	d)	What is the necessary and sufficient condition for linear phase Characteristics in FIR filter?	[4M]
	e)	Explain the term up sampling and down sampling.	[3M]
	f)	What are the different stages in pipelining?	[4M]

PART -B

2	a)	A system has unit sample response h(n) given by h(n)=-1/δ(n+1)+1/2δ(n)-1-1/4 δ(n-1). Is the system BIBO stable? Is the filter causal? Justify your answer	[8M]
	b)	Give the frequency domain representation of discrete time signals and systems.	[8M]
3	a)	How is the FFT algorithm applied to determine inverse discrete Fourier transform?	[8M]
	b)	Derive the equation to implement a butterfly structure In DIFFFT algorithm	[8M]
4	a)	Obtain the direct form I, direct form II and Cascade form realization of the following system functions. Y(n) = 0.1 y(n-1) + 0.2 y(n-2) + 3x(n) + 3.6 x(n-1) + 0.6 x(n-2).	[8M]
	b)	Prove that FIR filter has linear phase if the unit impulse response satisfies the condition h(n)=h(N-1-n), n=0,1,……M-1. Also discuss symmetric and antisymmetric cases of FIR filter.	[8M]
5	a)	Determine H(Z) for a Butterworth filter satisfying the following specifications: $0.8 \le \lvert H(e^{j\omega}) \rvert \le 1$, for $0 \le \omega \le \pi/4$ $\lvert H(e^{j\omega}) \rvert \le 0.2$, for $\pi/2 \le \omega \le \pi$ Assume T= 0.1 sec. Apply bilinear transformation method	[8M]
	b)	Use bilinear transformation method to obtain H(Z) if T= 1 sec and H(s) is 1/(s+1)(S+2) , 1/(s2+√2 s +1).	[8M]
6	a)	With necessary derivation explain the operation of sampling rate conversion by a non integer.	[8M]
	b)	The sequence x(n) = [0,3,6,9] is interpolated using interpolation sequence bk=[1/3, 2/3,1,2/3,1/3] and the interpolation factor of 3. Find the interpolated sequence y (m).	[8M]
7	a)	Explain Memory Access schemes in DSPs.	[8M]
	b)	Explain the memory interface block diagram for the TMS 320 C5x processor.	[8M]

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III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Find the power of the given signal below? [4M]

$$x[n] = \begin{cases} 3(-1)^n, & n \geq 0 \\ 0 & n < 0 \end{cases}$$

b) Compare overlap-add method and overlap-save method [4M]

c) Compare direct form I and direct form II realization of IIR systems. [4M]

d) What conditions are to be satisfied by the impulse response of an FIR system in order to have a linear phase? [3M]

e) What is the need for multirate signal processing? [3M]

f) What are the differences between fixed type processors and floating type processors? [4M]

PART –B

2 a) Find the solution to the following linear constant coefficient difference equation [10M]

$$y(n) - \frac{3}{2}y(n-1) + \frac{1}{2}y(n-2) = \left(\frac{1}{2}\right)^n \text{ for } n \geq 0$$

With initial conditions y(-1) = 4 and y(-2) = 10.

b) Derive the relationship between impulse response and frequency response of a discrete time system. [6M]

3 a) Compute the DFT of the sequence x(n) = sin[nπ/4], where N=8 using DIT FFT algorithm [8M]

b) Determine the IDFT of the sequence [8M]

$$X(K) = (6, -\sqrt{2} - j4.8284, -2 + j2, \sqrt{2} - j0.8284, -2, \sqrt{2} + j0.8284, -2 - j2, -\sqrt{2} - j4.8284$$

4 Obtain the cascade and parallel realisation structures for the following signals. [16M]

$$H(z) = \frac{2(1 - z^{-1})(1 + \sqrt{2}z^{-1} + z^{-2})}{(1 + 0.5z^{-1}(1 - 0.9z^{-1} + 0.81z^{-2}))}$$

Code No: RT32042 **R13** SET - 1

5 a) The desired frequency response of a low pass filter is [10M]

$$H_d(e^{jw}) = \begin{cases} e^{-j3w} & -\frac{3\pi}{4} \le w \le \frac{3\pi}{4} \\ 0 & \text{elsewhere} \end{cases}$$

Determine $H(e^{jw})$ for M =7 using a rectangular window.

b) What are the effects of windowing? [6M]

6 a) Derive an expression for the spectrum of output signal of an decimator. [8M]

b) What are the applications of multirate system? [8M]

7 a) What is MAC? Explain its operation in detail. [10M]

b) What are the various addressing modes used in the TMS320C5X processor? [6M]

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III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Show that the following systems are nonlinear and time invariant. [4M]
$y(n) - x(n)y(n-1) = x(n)$

b) Write computation efficiency of FFT over DFT. [3M]

c) What are the basic building blocks of realization structures? [4M]

d) Obtain the mapping formula for the impulse invariant transformation. [4M]

e) Write some examples of multirate digital systems. [3M]

f) What are the advantages of DSP processors in relation to general purpose processors? [4M]

PART –B

2 a) Determine the frequency response, magnitude and phase responses and time delay of the systems given by [10M]

$$y(n) - \frac{1}{2}y(n-1) = x(n)$$

b) Explain causality and stability of a linear time invariant system. [6M]

3 a) Find the DFT of the following sequence using FFT DIF? [8M]
X(n) = {1,2,3,5,5,3,2,1}

b) Compute the DFTs of the sequence $x(n) = 2^{-n}$, where N = 8 using DIT algorithm [8M]

4 Develop the cascade and parallel forms of the following causal IIR transfer functions. [16M]

$$H(z) = \frac{(3 + 5z^{-1})(0.6 + 3z^{-1})}{(1 - 2z^{-1} + 2z^{-2})(1 - z^{-1})}$$

5 a) Convert the analog filter to a digital filter whose system function is [10M]

$$H(s) = \frac{1}{(s+2)^2 + (s+1)}$$

Use bilinear transformation.

b) What is a Kaiser window? In what way is it superior to other window functions? [6M]

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6	a)	Draw the block diagram of a multistage interpolator and explain it	[8M]
	b)	A one stage decimator is characterized by the following Decimator factor = 3. Anti-aliasing filter coefficients h(0) = -0.06 = h(4), h(1)=0.3 =h(3), h(2) =0.62. Given the data, s(n) with successive values [6,-2,-3,8,6,4,-2], calculate and list the filtered output and the output of the decimator	[8M]
7	a)	Draw and explain the memory architecture of the TMS320C3X processor.	[10M]
	b)	What are the major advantages of having on-chip memory?	[6M]

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III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Show that the following system is nonlinear and time invariant. [4M]
$y(n+2) + 2y(n) = x(n+1) + 2$

b) State all properties of DFT [4M]

c) Distinguish the canonic and non-canonic structures. [4M]

d) Discuss the stability of the impulse invariant mapping technique. [3M]

e) What is meant by aliasing? How to avoid it? [4M]

f) List the basic characteristics of digital signal processor. [3M]

PART –B

2 a) Determine the frequency response, magnitude and phase responses and time delay of the systems given by [10M]
$y(n) = x(n) – x(n-1) + x(n - 2)$

b) State and explain the transfer function of an LTI system. [6M]

3 a) Find the N-point DFT for $x(n) = a^n$ for $0 < a < 1$? [8M]

b) Given $x(n) = \{1,2,3,4,4,3,2,1\}$, find X(k) using DIF FFT algorithm. [8M]

4 Realize the following IIR system functions in the direct form I and II and also parallel form. [16M]

$$H(z) = \frac{1}{(1 + az^{-1})(1 — bz^{-1})}$$

5 a) Design a digital Butterworth filter that satisfies the following constraint using bilinear transformation. Assume T=1sec. [10M]

$$0.9 \le |H(e^{jw})| \le 1 \qquad 0 \le w \le \frac{\pi}{2}$$

$$|H(e^{jw})| \le 2 \qquad \frac{3\pi}{4} \le w \le \pi$$

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b) What is a Hamming window function? Obtain its frequency domain characteristics. [6M]

6 a) Draw the block diagram of a multistage decimator and explain it [8M]

b) Discuss the computationally efficient implementation of decimator in an FIR filter. [8M]

7 a) Draw and explain the major block diagram of the TMS320C3X. [10M]

b) Explain the function of Barrel Shifter in the digital signal processor. [6M]

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DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) What isBIBO stability? What are the conditions for BIBO system? [4M]

b) How FFT is more efficient to determine DFT of sequence? [3M]

c) Distinguish between the methods of realization namely, block diagram representation and signal flow graph for implementing the digital filter transfer function. [4M]

d) What is the impulse invariant technique? [4M]

e) What are the drawbacks in multistage implementation? [3M]

f) Mention various generations of digital signal processors. [4M]

PART –B

2 a) Determine frequency, magnitude and phase responses and time delay for the system. [10M]

$$y(n) + \frac{1}{4}y(n - 1) = x(n) - x(n - 1)$$

b) Define the terms : linearity, time invariance and causality for a discrete time system. [6M]

3 a) Compute the FFT for the sequence x(n) = n+1 where N =8 using DIT algorithm [8M]

b) State and prove the periodicity property in DFT. [8M]

4 Realize the following IIR system functions in the direct form I and II and also parallel form. [16M]

$$H(z) = \frac{1}{(1 - az^{-1})^2} + \frac{1}{(1 - bz^{-1})^2}$$

5 a) What are the requirements for converting a stable analog filter into a stable digital filter? [6M]

Code No: RT32042 **R13** SET - 4

b) The desired frequency response of a low pass filter is [10M]

$$H_d(e^{jw}) = \begin{cases} 1; & -\frac{\pi}{2} \le w \le \frac{\pi}{2} \\ 0; & \frac{\pi}{2} \le w \le \pi \end{cases}$$

Determine $h_d(n)$ for M =7 using a rectangular window.

6 a) How can sampling rate be converted by a rational factor M/L? [8M]

b) Draw and explain the polyphase structure of a interpolator. [8M]

7 a) Explain the purpose of six registers used in the TMS320C2X processor. [10M]

b) What are the limitations of pipelining in Digital Signal Processor? [6M]

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